AMENDMENTS TO THE SPECIFICATION

Please amend paragraph [0018] as follows:

[0018] Figures 10A and 10B are ~~is a~~ schematic block diagrams of the parallel to serial module in accordance with the present invention; and

Please amend paragraph [0027] as follows:

[0027] Figure 3 is a schematic block diagram of the programmable transmit PMA module 38 that includes a programmable serializing data path 80 and a line driver 89. The programmable serializing data path 80 includes a programmable timing circuit 82, which will be described in greater detail with reference to Figures 4 - 9, and a parallel to serial module 84, which will be described in greater detail with reference to Figures 4, 10A, and 10B. In general, the programmable timing circuit 82 is operably coupled to generate a first plurality of timing signals when width 87 of parallel input data 48 is of a first multiple and to generate a second plurality of timing signals when the width 87 of the parallel input data is of a second multiple. The parallel to serial module 84 is operably coupled to convert the parallel input data 48 into serial output data 86 based on the first or second plurality of timing signals 88. The line driver 89 is operably coupled to drive the serial output data 86 onto a transmission line as the transmit serial data 50.

Please amend paragraph [0031] as follows:

[0031] The first multiplexing module 96, which will be described in greater detail with reference to Figures 10A and 10B, is operably coupled to receive the transmit parallel data 48 and, based on the first or second parallel data clock 106, produce n-bit first intermediate data 102. In one embodiment, the first multiplexing module 96 includes four 16 to 1 multiplexers that collectively convert transmit parallel data into a four bit data stream.

Please amend paragraph [0044] as follows:

[0044] Figure 10A is a schematic block diagram of an embodiment of the parallel to serial module 84. In this embodiment, the parallel to serial module 84 includes four 16 to 1 multiplexers for the first multiplexing module 96, two 2 to 1 multiplexers 142 and 144 for the second multiplexing module 98, and one 2 to 1 multiplexer for the third multiplexing module 100. Note that the four 16 to 1 multiplexers of the first multiplexing module 96 are shown superimposed such that the zeroth bit position of the first multiplexing module 96 receives bits 0 through 3 [3:0] of the parallel data 48. In this configuration, a first one of the four 16 to 1 multiplexers receive bit 0, a second multiplexer receives bit 1, a third multiplexer receives bit 2, and the fourth multiplexer receives bit 3.

Please insert the following new paragraph after paragraph [0048] and prior to paragraph [0049]:

[0048.1] Figure 10B is a schematic block diagram of an embodiment of the parallel to serial module 84. This embodiment is similar to the embodiment shown in Figure 10A with the addition of input latches 161, 162, and 163 at the inputs to multiplexing modules 96, 142, and 144, respectively, and output latch 164 at the output of multiplexing module 96. These latches may be used to temporarily store data.